REMARKS/ARGUMENTS

Claim 1 was rejected as being unpatentable over Thurber, Jr. (U.S. Patent No. 6,169,444). Applicant traverses this rejection.

The charge pump circuit of the present invention includes a delay circuit (B1; Fig. 3) to increase the voltage conversion efficiency. As shown in Fig. 4 of the present specification, after a gate voltage (φT1) of a first transistor (TR1) is determined to be at a low level sufficient to turn off the first transistor and the first transistor changes its state from an ON state to an OFF state, the delay circuit (B1) delays the determined voltage (φT1) and generates a delayed signal (φC1), thereby decreasing a voltage of the node (N1) between the first and second transistors (TR1, TR2) to the low level. That is, the voltage at the node (N1) changes after the gate voltage is determined to be at the low level that turns off the transistor (TR1). In other words, the node N1 voltage does not change while the gate voltage is decreasing, which prevents a large through current from flowing through the first and second transistors (TR1, TR2).

The Examiner states that switches S2 and S4 of Fig. 4 of Thurber correspond to a delay circuit of the present invention because it is inherent that any semiconductor element has a delay. However, the inherent delay of the semiconductor element cannot cause a voltage at the node between the switches (S2-S4) to change by changing the state of the switch S4 after the switch S1 changes to an OFF state. Accordingly, it is not possible to prevent a large through current from flowing through the switches S2 and S4. In other words, the switches S2 and S4 operate substantially simultaneously even if they have the inherent delay, and the inherent delay of the semiconductor element is just a prior art of the present invention.

Furthermore, Thurber discloses providing a clock signal to the switches S3 and S4 via an inverter. However, even if the inverter delays the clock signal, Thurber's circuit of Fig. 4 cannot obtain the advantage of the present invention for the following reasons.

In Fig. 4 of Thurber, though there is no detailed description regarding the operation of the switches S1-S4, it appears that switches S1 and S2 operate substantially simultaneously and switches

S3 and S4 operate substantially simultaneously because S1 and S3 are connected to S2 and S4, respectively.

Assuming that the switches S1 and S3 are turned on and the switches S3 and S4 are turned off, when the switches S1 and S2 are turned off there is a state where all the switches S1-S4 are instantaneously turned off because a clock signal provided to the switches S3 and S4 is delayed. Then, the switches S3 and S4 are turned on in response to the delayed clock signal, thereby charging a boosted voltage 2V-IN in a capacitor C-X.

In contrast, assuming that switches S1 and S2 are turned off and switches S3 and S4 are turned on, when the switches S1 and S2 are turned on there is a state where all the switches S1-S4 are instantaneously turned on because a clock signal provided to the switches S3 and S4 is delayed. At this time, a voltage V-OUT is fixed to the voltage V-IN. Then, the switches S3 and S4 are turned off in response to the delayed clock signal, thereby charging a voltage V-IN in a capacitor C-OUT. That is, a boosted voltage 2V-IN cannot be obtained in this case.

Accordingly, a boosted voltage cannot be stably generated when using an inverter having a delay, and the Thurber's circuit cannot obtain the advantage of the present invention.

As discussed above, Thurber does not teach or suggest that the delay circuit delays the first clock signal and provides the delayed first clock signal to the second terminal of the capacitor such that the second transistor changes its state later than the timing at which the first transistor change its state from an ON state to an OFF state as recited in claim 1. In other words, Thurber cannot provide a delayed clock signal to the terminal of the capacitor C-X (the node between the switches S2 and S4) such that the switch S4 changes its state later than the timing at which the switch S1 or S2 changes its state from an ON state to an OFF state using the inverter. Accordingly, the switches S2 and S4 of Fig. 4 of Thurber do not correspond to the delay circuit of the present invention, and the present invention is not obvious over Thurber.

Claims 2, 3, 6 and 9 were rejected as being unpatentable over Thurber, Jr. in view of Mukainakano et al. (U.S. Patent No. 6,107,862, hereinafter "Mukainakano"). Applicant traverses this rejection.

Since neither Thurber nor Mukainakano discloses the delay circuit of the present invention, we believe that the present invention of claims 2, 3, 6, and 9 is not obvious over Thurber in view of Mukainakano.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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